## AMENDMENTS TO THE CLAIMS

- 1. (Original) A method, comprising:
  - receiving accelerated graphics port (AGP) transaction requests at a first bus interface from a core logic device;
  - buffering the received AGP transaction requests using a request queue coupled to the first bus interface;
  - exchanging the AGP transaction requests using a second bus interface for access to the first bus interface between the core logic device and a graphics controller; and
  - arbitrating access to the first bus interface using a request arbiter coupled to the second bus interface.
- initiating data transactions by the graphics controller, and receiving data

(Original) The method of claim 1, further comprising:

transactions initiated by the core logic device using a third bus interface;

exchanging the AGP transaction requests for access to the second bus interface

between the core logic device and the graphics controller; and

arbitrating access to the second bus interface using a data transaction arbiter

- coupled to the third bus interface.
- 3. (Original) The method of claim 2, further comprising:

initiating data transactions by the graphics controller, and receiving data

transactions initiated by the core logic device using a fourth bus interface;

exchanging the AGP transaction requests for access to the third bus interface

between the core logic device and the graphics controller; and

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arbitrating access to the third bus interface using a data transaction arbiter coupled to the fourth bus interface.

- 4. (Original) The method of claim 1, further comprises implementing a common, distributed arbitration mechanism using the request arbiter and a corresponding request arbiter of the core logic device.
- 5. (Original) A system, comprising:
  - a storage medium;
  - a processor coupled with the storage medium; and
  - a graphics controller coupled to the storage medium and the processor, the graphics controller having
    - a first bus interface to receive accelerated graphics port (AGP) transaction requests from a core logic device;
    - a request queue coupled to the first bus interface to buffer received AGP transaction requests;
    - a second bus interface to exchange requests for access to the first bus interface between the core logic device and a graphics controller; and
    - a request arbiter coupled to the second bus interface to arbitrate access to the first bus interface.
- 6. (Original) The system of claim 5, wherein the graphic controller further comprising:
  - a third bus interface to initiate data transactions by the graphics controller and to receive data transactions initiated by the core logic device;

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- a fourth bus interface to exchange requests for access to the third bus interface
  between the core logic device and the graphics controller; and
  a data transaction arbiter coupled to the fourth bus interface to arbitrate access to
  the fourth bus interface.
- 7. (Original) The system of claim 6, wherein the request arbiter of the core logic device is to implement a common, distributed arbitration mechanism.
- 8. (Original) A graphics controller, comprising:
  - a first bus interface to receive accelerated graphics port (AGP) transaction requests from a core logic device;
  - a request queue coupled to the first bus interface to buffer received AGP transaction requests;
  - a second bus interface to exchange requests for access to the first bus interface
    between the core logic device and a graphics controller; and
    a request arbiter coupled to the second bus interface to arbitrate access to the first
    bus interface.
- 9. (Original) The graphics controller of claim 8, further comprising:
  a third bus interface to initiate data transactions by the graphics controller and to
  receive data transactions initiated by the core logic device;
  a fourth bus interface to exchange requests for access to the third bus interface
  between the core logic device and the graphics controller; and

a data transaction arbiter coupled to the fourth bus interface to arbitrate access to the fourth bus interface.

Docket No.: 42390P6727C2 Application No.: 10/785,281 10. (Original) The graphics controller of claim 8, wherein the request arbiter of the core logic device is to implement a common, distributed arbitration mechanism.

Claims 11. – 18. (Cancelled)

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